REMARKS

Applicants appreciate the recognition of patentable subject matter in the present application and the withdrawal of the previous prior art rejections.

Applicants hereby add new claims 123-131. Accordingly, claims 74, 75, 77-86, 88-89, 92-94, 96, 102-106, 108, 109, 111, 113, 114, 116, 118 and 120-131 are pending in the present application. .

Claim 79 stands rejected under 35 USC 102(e) for anticipation by U.S. Patent No. 6,417,605 to Hoffmann et al. Claims 83-85, 88-89, 92, 116 and 121 stand rejected under 35 USC 102(e) for anticipation by U.S. Patent No. 6,020,595 to Itoh et al. Claims 93-94 and 96 stand rejected under 35 USC 102(e) for anticipation by U.S. Patent No. 5,962,894 to Gardner et al. Claim 80 stands rejected under 35 USC 103 for obviousness over Hoffman in view of U.S. Patent No. 6,163,107 to Itoh et al. Claims 114 and 122 stand rejected under 35 USC 103 for obviousness over Itoh '107 in view of U.S. Patent No. '595 to Itoh.

Applicants respectfully request reconsideration of the rejections.

Referring to independent claim 79, the Office relies upon teachings of cols. 8-9 of Hoffman as allegedly teaching the claimed *self-aligning of the gate with the semiconductive regions*. Hoffman teaches gate 17a intermediate regions 19a, 19b. The self-alignment teachings of cols. 8-9 refer to an extraction grid 15 (col. 7, line 46) separate from gate 17a. The self-alignment of reference 15 fails to teach or suggest *self-aligning of the claimed*

*gate with the **plurality of semiconductive regions** which are adjacent to the channel region of the semiconductive material.* Applicants have failed to uncover any teachings of self-alignment of gate 17a with regions 19a, 19b in Hoffman.

More spefically, claim 79 recites a *field effect transistor fabrication method* comprising providing *plural semiconductive regions* and *self-aligning the gate with the **plural semiconductive regions***. The teachings of col. 9 of Hoffman (as well as U.S. Patent No. 5,372,973 identified in col. 9 with respect to the self-alignment) refer to self-alignment of a conductor with respect to the emitter of the cathode and fail to teach or suggest the claimed *self-alignment of the gate with plural semiconductive regions during the fabrication of the transistor* as claimed.

The alignment of the gate with one emitter fails to teach or suggest the transistor fabrication method of self-aligning the gate with the plurality of semiconductive regions. The alignment of Doan with the emitter 13a of the single semiconductive region 19b referred to in col. 9 of Hoffman fails to teach or suggest self-alignment of a gate with a plurality of semiconductive regions. The self-alignment of reference15 with the emitter 13a of only one of the semiconductive regions 19b of the transistor fails to teach or suggest the claimed *self-alignment of the gate with the plurality of semiconductive regions* of the transistor fabrication method as positively defined in claim 79. Applicants respectfully submit that positively recited limitations of claim 79 are not disclosed nor suggested by the prior art and claim 79 is allowable for at least this reason.

The claims which depend from independent claim 79 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to the rejection of dependent claim 80, Applicants respectfully submit the rejection is improper under 103(c) and claim 80 is allowable. In particular, Hoffman and the present application were commonly owned at the time the claimed invention was made. Applicants respectfully submit that the 103 rejection over Hoffman is improper under 103(c) inasmuch as Hoffman only qualifies as prior art under 102(e). See MPEP 706.02(l)(8th ed., rev. 5). Applicants respectfully request withdrawal of the 103 rejection of claim 80 in the next Action for at least this reason.

Referring to independent claim 83, the method recites *providing a plurality of semiconductive regions* and *wherein one of the semiconductive regions comprises a plurality of emitters*. At page 3 of the Action, the Office identifies regions of layer 5 adjacent to the channel region as allegedly teaching the claimed providing the semiconductive regions. However, at col. 6, lines 33+ of Itoh '107, it is stated that the remaining portions of ***electrode 5*** (those portions not above electrode 3) are formed with ***high conductivity*** as distinguished from the portion of 5 above the electrode 3. Itoh '107 accordingly discloses both conductive materials (portions of 5 not above the electrode 3) and semiconductive material (portion of 5 above the electrode 3). Applicants respectfully submit that the *high conductivity portions of the* ***electrode 5*** fail to teach or suggest the

plurality of semiconductive regions as positively claimed.

The claims which depend from independent claim 83 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, referring to dependent claim 85, the Office merely cites "Fig. 1" as allegedly teaching the claimed *field effect transistor*. Applicants have electronically searched Itoh and failed to uncover any disclosure that the arrangement of Fig. 1 is a field effect transistor. To the contrary, Itoh clearly refers to FETs at col. 12, lines 55+ with respect to embodiments different from Fig. 1. Applicants respectfully submit that the limitations of claim 85 are not disclosed by Itoh for the above-mentioned compelling reasons and claim 85 is allowable.

Referring to independent claim 89, Applicants respectfully submit that the *high conductivity portions of electrode 5* (relied upon by the Office on page 3 of the Action) fail to teach or suggest the claimed limitations of *providing the plurality of semiconductive regions adjacent to a channel region* as claimed. Applicants respectfully submit that positively-recited limitations of the claims are not disclosed nor suggested by the prior art and the rejection is improper for at least this reason.

The claims which depend from independent claim 89 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to dependent claim 92, Applicants have failed to uncover any teaching in Itoh of Fig. 1 disclosing a *field effect transistor* as positively claimed. Claim 92 is allowable.

Referring to independent claim 93, the Office relies upon the teachings of Fig. 1J of Gardner in support of the rejection. Col. 7, lines 44+ of Garner state that surface 138 is above surface 104 as is also clearly depicted in Fig. 1J. The different elevations of surfaces 104, 138 fail to teach or suggest the claimed *upper surfaces of the semiconductive regions being elevationally coincident with the upper surface of the gate.* Positively recited limitations of claim 93 are not disclosed nor suggested by the prior art and claim 93 is allowable for at least this reason.

The claims which depend from independent claim 93 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to independent claim 116, the method recites providing a source semiconductive region and a drain semiconductive region. The Office on page 4 of the Action identifies reference 4 of Itoh '107 as allegedly teaching the claimed providing the source semiconductive region. At col. 6 of Itoh '107, it is clear that reference 4 refers to ***an electrode***. The Office has failed to identify any teachings of Itoh that electrode 4 may be fairly considered to teach a semiconductive region as claimed. Limitations of claim 116 are not disclosed nor suggested by the prior art and claim 116 is allowable for at least this reason.

The claims which depend from independent claim 116 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Applicants add new claims 123-131 which are supported at least by Figs. 12, 16 and 17 and the associated teachings of the specification.

Applicants respectfully request allowance of the claims for at least the above-mentioned compelling reasons.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 1/8/07

By: _____
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